

Notice of References Cited	Application/Control No. 09/976,298	Applicant(s)/Patent Under Reexamination MAGEN, MICHA	
	Examiner Mark Connolly	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

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*	A	US-5,195,111	03-1993	Adachi et al.	377/52
*	B	US-4,315,166	02-1982	Hughes, John B.	377/33
*	C	US-4,179,670	12-1979	Kingsbury, Nicholas G.	331/10
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	M	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Foroudi et al., Low-voltage low-power topology for high-speed applications, 2001, IEEE, pgs 135-138.
	V	Nelson Victor P et al., Digital Logic Circuit Analysis and Design, 1995, Prentice Hall Inc., pgs 449-477.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.